Docket No.: W&B-INF-952

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German Application No. 100 63 627.6

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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W&B-INF-952

Description

Integrated circuit having a data processing unit and a buffer memory

The invention relates to an integrated circuit having a data processing unit and a buffer memory.

An integrated circuit is conventionally tested by the integrated circuit being supplied with test data by a tester. The output values obtained depending on the applied test data are transferred back to the tester and checked there. If the tester ascertains that a value that has been transferred back does not correspond to a desired value, a defect is identified.

To repair defects in integrated circuits, provision is often made of setting memories which are written to after the conclusion of a test in order e.g. to disconnect defective circuit areas and replace them by redundant circuit elements that are additionally provided on the integrated circuit. This is done by using so-called fuses, which represent switches which are initially closed or open and are then opened or closed, respectively, depending on the setting to be performed, with the aid of a suitable programming circuit.

The calculation of the required settings is conventionally carried out in an external tester. This procedure is very time-intensive in particular on account of the data transfer from and to the tester. If it is desired to determine the settings that are to be performed in the tested integrated circuit, then it is necessary to provide an integrated

processing circuit including register memories in which the settings are calculated. In the case of memory modules, this processing circuit would have to optimize the settings that are to be performed by means of a redundancy calculation, the settings then activating replacement elements for defect addresses in a memory array. The redundancy calculation in the processing unit is usually carried out by an iterative method. Determining corresponding settings in the circuit to be tested has the disadvantage that a considerable additional outlay on circuitry would be necessary for the processing circuit which carries out the redundancy calculation.

It is an object of this invention, therefore, to provide an integrated circuit with which it is possible to determine the individual settings for the setting memory, the required outlay on circuitry being minimized.

This object is achieved by means of the integrated circuit according to claim 1. Further advantageous embodiments are specified in the dependent claims.

The invention provides an integrated circuit having a data processing unit, a buffer memory and a setting memory. The buffer memory contains registers for the data processing unit. The buffer memory is connected to the setting memory, the setting memory being able to be written to and/or read from via the buffer memory.

This invention has the advantage that it is possible to perform a redundancy calculation for determining the setting values for the setting memory in the integrated circuit which is tested. The requisite circuit, which has a data processing unit, a buffer memory and a setting memory, in order to carry out the required calculations, would have a non-negligible

area requirement in the integrated circuit on account of the outlay on circuitry for the register memory. The additional area requirement can be minimized by virtue of the fact that the invention provides for the buffer memory that is available anyway in the integrated circuit for writing to the setting memories also to be used as a register for a data processing unit. All that is necessary is an additional outlay on circuitry for the processing unit, but not for the register memories.

In a further preferred embodiment, it is provided that the integrated circuit has circuit elements for replacing defective circuit areas, the circuit elements being able to be activated by the setting memory. The circuit elements are preferably memory elements which replace defective memory areas of a memory. In this case, it is particularly advantageous to perform the determination of the settings in the integrated circuit to be tested, since, in particular, the optimal utilization of the available circuit elements which are intended to replace the defective memory areas can be calculated only with some computation complexity. The requisite settings are usually determined iteratively, i.e. in a computationally intensive approximation method. With the apparatus according to the invention, it is possible to carry out the requisite computation operations in parallel in the respective integrated circuit, thereby making it possible to save computation capacity in a tester.

In accordance with a further preferred embodiment, it is provided that the processing unit has an arithmetic logic unit (ALU). Such an arithmetic logic unit is usually constructed so that coded instructions in a program memory are applied to the contents of one or more registers. Furthermore, it is provided that the buffer memory of the integrated circuit is subdivided

into a plurality of registers, at least one register being provided for the data to be processed and a further register being provided for coded instructions for the ALU. In this case, the integrated circuit preferably has two data registers for the data to be processed. Such a configuration is advantageous in order that a program register for the coded instructions and two data registers are provided, with whose contents arithmetic or logical operations can be executed in accordance with the instructions. The result is written back to one of the data registers. Since the data can be written to the register cells via the arithmetic logic unit, it is possible for the ALU to write the determined settings directly to the relevant position of the buffer memory for the setting memory. A considerable amount of time can be saved in this way, since the transfer of determined data from the integrated circuit to the tester and/or vice versa is obviated.

The invention is explained in more detail with reference to the accompanying drawing, in which:

Figure 1 shows a block diagram of an integrated circuit in accordance with an embodiment of the invention.

Figure 1 schematically shows a block diagram of an integrated circuit in accordance with a preferred embodiment of the invention. A setting memory 1 with setting memory cells 2 is situated in an integrated circuit (not shown). The setting memory 1 serves for activating redundant circuit areas, in particular redundant memory areas, in order thereby to replace defective areas of a memory array (not shown). The setting memory 1 is connected to a latch 3 with latch cells 4, so that each setting memory cell 2 is assigned a latch cell 4. The latch 3 is subdivided into a first latch area 5, a second latch area 6 and a third latch area 7, the latch cells 4 in

each of the latch areas 5, 6, 7 being connected up as shift registers, i.e. the output of one latch cell is connected to the input of a next latch cell 4. The first latch area 5 and the second latch area 6 preferably have the same number of latch cells 4 in each case. However, it may also be provided that the number of latch cells 4 in the first latch area 5 differs from that in the second latch area 6.
The respective first and last latch cells of the latch cells 4 of the three latch areas 5, 6, 7 are provided with the reference symbols 41, 43, 45 and 42, 44, 46, respectively. The output of the last latch cell 42 of the first latch area 5 is switchably connected via a switch S1 to the input of the first latch cell 43 of the second latch area 6, so that a shift register comprising the first and second latch areas is formed when the switch is closed. Equally, the output of the last latch cell 44 of the second latch area 6 is switchably connected via a switch S2 to an input of the first latch cell 45 of the third latch area 7, so that a shift register is formed by means of the second latch area 6 and the third latch area 7 when the switch S2 is closed. If both switches S1 and S2 are closed, all the latch cells 4 together form a shift register.

The outputs of the last latch cells 42, 44 of the first latch area 5 and of the second latch area 6 are in each case connected to a processing unit 8, so that the data in the latch areas 5, 6, 7 can be read serially. An output of the processing unit 8 is connected to an input of the first latch cell 41 of the first area 5. The output of the last latch cell 46 of the third latch area 7 is connected, on the one hand, to an input of the processing unit 8 and is switchably connected, on the other hand, via a switch S3 to the input of the first latch cell 45 of the third latch area 7. The switches S1, S2 and S3 are controlled via the processing unit 8. Furthermore,

an external tester (not shown) is connected to the input of the first latch cell 41 of the first area 5, via which tester the latch cells can be written to or read from.

In order to generate setting data for the setting memory 1 from defect data, i.e. defective output data given the presence of a specific test pattern, such as e.g. addresses of defective memory cells, the defect data must usually be processed in an algorithm. The result of the algorithm then constitutes setting data which are stored in the setting memory 1. In conventional test systems, this calculation is carried out in an external tester (not shown), i.e. the defect data are transferred to the external tester, where the calculation is carried out, and then the setting data are transferred back into the integrated circuit for storage in the setting memory 1.

In the present exemplary embodiment, the integrated circuit is provided in a memory module. After being written to, the setting memory 1 then receives setting values, whereby redundancy memory areas are enabled which replace defective memory cells in a main cell array. Since both word and bit lines and individual cells can be replaced by the setting memory, it is expedient to combine, in an algorithm, defective cells, if possible, to form word or bit lines which are then replaced by a redundant word or bit line provided therefor.

The integrated circuit according to the invention makes it possible to carry out this calculation in the memory module. As a result of using the latch cells 4 for the setting memory cells 2 as registers for the processing unit 8, a considerable amount of area can be saved on the memory module.

A redundancy calculation is carried out as follows: firstly the determined defect data and the processing instructions are made available by the tester (not shown) and are then written serially to the latch 3, designed as a shift register, so that the first latch area 5 and the second latch area 6 contain defect data and the third latch area 7 contains instruction data. In order to write these data to the latch 3, the switches S1 and S2 must be closed, so that the entire latch 3 forms a uniform shift register. However, data which are generated in the integrated circuit or are stored there can also be written to the latch 3. Thus, by way of example, data from a desired/actual comparison which takes place in the integrated circuit can be written to the latch areas 5, 6 and program data from a ROM memory can be written to the latch area 7.

If the latch 3 contains the data provided, the processing unit 8 begins to execute the instruction in the third latch area 7. To that end, the switches S1 and S2 are opened and switch S3, depending on whether cyclic processing is necessary, is closed. The content of the last latch cell 46 of the third area 7 is then read out by being shifted toward the right into the processing unit 8. In this case, the content of the last latch cell 46 is written to the first latch cell 45 of the third latch area 7 again if the switch S3 is closed.

In accordance with the received instruction, the processing unit 8 reads in the content of the last latch cell 42 of the first latch area 5 and/or the content of the last latch cell 44 of the second latch area 6 and combines these contents in accordance with the received instructions. The result is written to the first latch cell 41 of the first latch area 5, and all of the positions of the latch cells 4 are shifted

toward the right, the content of the last latch cell 42 of the first latch area being read into the processing unit 8.

This processing cycle is repeated a predetermined number of times and, in the process, successively through a shifting-toward-the-right of the latch cells of the first area 5 and/or of the latch cells 4 of the second latch area 6, all the latch cells of the first latch area 5 and of the second latch area 6 are processed in accordance with the received instruction in the processing unit 8. With the read-out of the contents of the latch cells 4 of the first latch area 5, the respective result of the processing is simultaneously written to the first latch area 5 at the input of the first latch cell 41 of the first latch area 5.

After the specific number of cycles has taken place, the instruction has been processed and the next instruction is read from the last latch cell 46 of the third latch area 7 into the processing unit by a shifting-toward-the-right process. In said unit, as described above, the content of the latch cells 4 of the first latch area 5 and/or the content of the latch cells of the second latch area 6 are/is processed in accordance with the instruction and the result is in each case written to the first latch cell 41 of the first latch area 5. The processes of read-out and writing to the latch area 5 and the second latch area 6 are effected by the contents being shifted toward the right.

The processing unit 8 can likewise provide, through control of the switch S1, for the contents of the first latch area 5 to be transferred into the second latch area 6 by a shifting-toward-the-right process. Analogously, it is also possible to transfer contents of the second latch area 6 via the processing unit 8 - controlled by instructions stored in the

third latch area 7 - into the first latch area 5. Furthermore, it is possible, by the closing of the switch S2 and opening of the switch S3, to transfer the content of the second latch area 6 into the third latch area 7. This means that it is also possible to load a result of a previously effected operation into the third latch area 7, the instruction memory, which means that it is possible to carry out complex program sequences which depend on the result of previous operations.

It may furthermore be provided that the integrated circuit according to the invention uses only some of the available latch cells 4 as register cells. By way of example, the output of the last latch cell 46 of the third area 7 could be connected via a further switch (not shown) to further latch cells 4 assigned to respective setting memory cells 2. As a result, it would be possible to store setting values already determined for the setting memory 1 in the relevant latch cells 4 without these values having to be transferred beforehand to the external tester for buffer-storage or the like.

It goes without saying that the latch cells 4 can also be subdivided into more than three areas. This means that it is possible to perform even more complex operations with more than two registers in the processing unit 8.

The closing of the switch S3 effects feedback of the program memory in the third latch area 7, so that a predetermined sequence of instructions can be executed repeatedly. This is preferably suitable for carrying out iterative calculation methods which have to be performed in particular in the optimization of setting values from defect data. This enables a considerable amount of computation time to be saved, since, during a test run, the integrated modules can carry out in

parallel computation operations which would have taken place in the tester according to a conventional method.

The size of the latch areas 5, 6, 7 can be chosen arbitrarily. It is expedient, however, to provide the first and second latch areas 5, 6 in the size of a memory address, in order to be able to process addresses of defective memory cells, and to provide the third latch area 7 in a size sufficient for the operations for the processing unit 8.

The features of the invention which are disclosed in the above description, the drawing and the claims may be of importance both individually and in any desired combination for the realization of the invention in its various configurations.

Patent claims

1. An integrated circuit having a data processing unit (8), a buffer memory (3), which contains registers (5, 6, 7) for storing data for the data processing unit (8), and a setting memory (1),
characterized in that
the buffer memory (3) is connected to the setting memory (1), the setting memory (1) being able to be written to and/or read from via the buffer memory (3).

2. The integrated circuit as claimed in claim 1, characterized in that the setting memory (1) serves for activating circuit elements.

3. The integrated circuit as claimed in claim 2, characterized in that the circuit elements to be activated are memory elements which replace memory areas of a memory.

4. The integrated circuit as claimed in one of claims 1 to 3, characterized in that the processing unit (8) comprises an arithmetic logic unit.

5. The integrated circuit as claimed in one of claims 1 to 4, characterized in that a register (5, 6) of the buffer memory (3) is provided for data to be processed and a further register (7) of the buffer memory (3) is provided for coded instructions for the arithmetic logic unit.

6. The integrated circuit as claimed in claim 5, characterized in that the integrated circuit has two buffer memories (3) which contain data to be processed.

7. The integrated circuit as claimed in one of the preceding claims, characterized in that the buffer memory (3) is designed as a latch.

8. The integrated circuit as claimed in one of the preceding claims, characterized in that the buffer memory (3) has a shift register.

9. The integrated circuit as claimed in claim 8, characterized in that the shift register has at least one switch (S1, S2), in order to subdivide the shift register into registers (5, 6, 7) for the processing unit (8).

10. The integrated circuit as claimed in one of the preceding claims, characterized in that the registers (5, 6, 7) can in each case be written to and read from serially by the processing unit (8).

11. The integrated circuit as claimed in one of the preceding claims, characterized in that the setting memory (1) contains electrical fuses.

12. The use of the integrated circuit as claimed in one of the preceding claims for determining setting data for the setting memory from address data, stored in a register, of memory areas of a memory that have been identified as defective, depending on instruction data stored in a register.

Abstract

Integrated circuit having a data processing unit and a buffer memory

The invention relates to an integrated circuit having a data processing unit (8), a buffer memory (3) and a setting memory (1). The buffer memory (3) performs the function of registers (5, 6, 7) for storing data for the processing unit (8). The buffer memory (3) is connected to the setting memory (1), the setting memory (1) being able to be written to via the buffer memory (3).

Figure 1

List of reference symbols

1	Setting memory
2	Setting memory cell
3	Latch
4	Latch cells
5	1st latch area
6	2nd latch area
7	3rd latch area
8	Processing unit
41-46	Latch cells
S1,S2,S3	Switches

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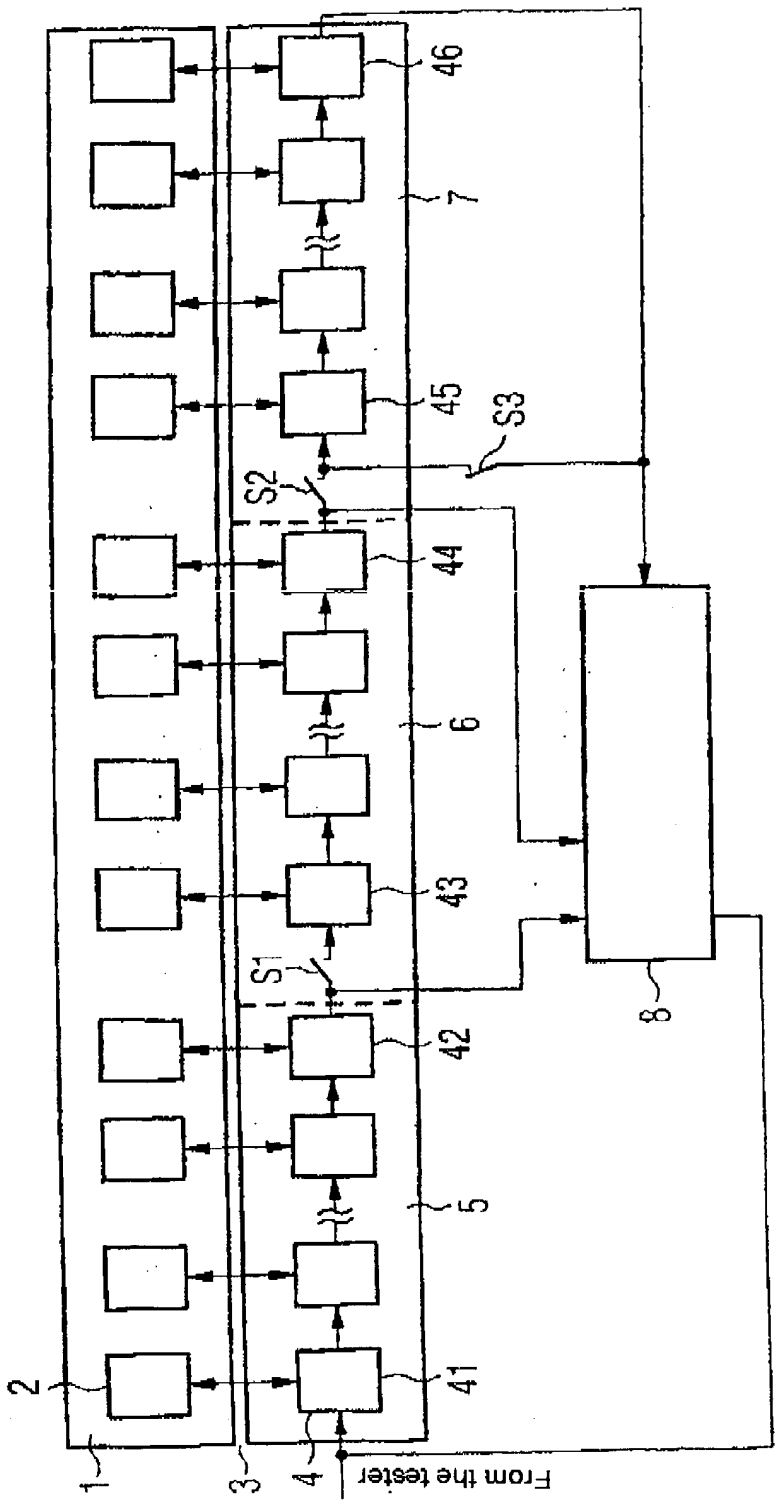

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